

A MULTI-RATE, MULTI-PORT, GIGABIT SERDES TRANSCEIVER

ABSTRACT OF THE DISCLOSURE

A multi-port Serdes transceiver includes multiple parallel ports and serial ports, and includes the flexibility to connect any one of the parallel ports to another parallel port or to a serial port, or both. Furthermore, the multi-port transceiver chip can connect any one of serial ports to another serial port or to one of the parallel ports. The substrate layout of the multi-port Serdes transceiver chip is configured so that the parallel ports and the serial ports are on the outer perimeter of the substrate. A logic core is at the center of the substrate, where the logic core operates the serial and parallel data ports, and the bus that connects the data ports. The bus can be described as a "ring" structure (or donut "structure") around the logic core, and is configured between the logic core and the data ports. The ring structure of the bus provides efficient communication between the logic core and the various data ports.